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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,185	08/06/2003	Theodore W. Houston	TI-35149	9273

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EXAMINER	
WEINBERG, MICHAEL J	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,185	HOUSTON, THEODORE W.	
	Examiner	Art Unit	
	Michael J. Weinberg	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-17, and 19-21* is/are rejected.

7)☒ Claim(s) *5,11,18 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03 & 1/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) received on 11/18/2003 and 1/24/2005 have been considered by the examiner. One reference was crossed out on the latter IDS because the citation is redundant.

Drawings

2. The new drawings submitted on 7/28/2006 would be acceptable if amended correctly. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Claim Objections

3. Claim 11 is objected to because of the following informalities:

With regard to claim 11, there is no antecedent basis for "said dummy bit line switching circuitry". The claim will be treated as if the phrase "dummy bit line" has been removed.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6-17, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naiki (US Patent 5,446,699) in view of Admitted Prior Art (APA).

With regard to **claim 1**, Naiki discloses an SRAM device, comprising:

a column of asymmetric memory cells (They have a "positional deviation". See col. 2, lines 6-14.) spanning opposing bit lines (bit line pairs 48 or 49 in fig. 9) in alternating orientations (See col 2, lines 6-36. Odd rows comprise one orientation while even rows comprise the other orientation.);

sensing circuitry (87 in figure 11, 81/82 in figure 10, *or* sensing circuitry is considered inherently connected to the data-line pair as discussed below) configured to sense stored values in said cells; (Selecting transistors are well-known to be for reading/sensing or writing. Thus they can be considered as sensing circuitry.)

switching circuitry (the decoder and logic gates in figures 10, 11, or 12 which inherently comprise switches) configured to adapt the sensing circuitry as a function of said orientations (ie a function of the LSB X1 of the row address as taught in col. 9, lines 22-31).

Naiki does not teach that the switching circuitry is associated with a sense amplifier component. However, sense amplifiers are well-known in the art as shown in

APA (paragraph 3 of the application) and could reasonably be connected to data line pairs such as the ones in figures 10, 11, or 12.

Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add a sense amplifier to the teachings of Naiki in order to accurately sense the values of the cells.

With regard to **claim 2**, Naiki further discloses an SRAM device as recited in claim 1 wherein said column has only two of said opposing bit lines. (See any of figures 9-11- They are bit line pairs.)

With regard **claim 3**, Naiki further discloses an SRAM device as recited in claim 1 wherein said switching circuitry (column decoder and logic gates) is configured to apply different voltage signals (Only one of Co or Ce in figure 10 or adjacent bit lines in other embodiments is high at a time) to opposing sides of said sensing circuitry. (See 82 of figure 10- Signal lines are connected to opposing sides.)

With regard to **claim 4**, Naiki further discloses an SRAM device as recited in claim 1 wherein said orientations alternate based on a power of two. (Even/odd, as shown in the abstract, fits this formula.)

With regard to **claim 6**, Naiki further discloses an SRAM device as recited in claim 1 wherein said switching circuitry (column decoder and logic gates) receives a signal X1 representing said orientations from a line (see Row address LSB in figures 10-12) of an address bus associated with said SRAM device.

With regard to **claim 7**, Naiki further discloses an SRAM device as recited in Claim 1 wherein said asymmetric memory cells in said column are of a number that is a

power of two. (This is shown in the background of the invention (col. 1) and associated figure 2 where capacities from 256 kilobits to 16 megabits are disclosed, all powers of two. Also see figure 2, where the number of word lines WL are 2^m. It is also considered obvious to vary the number of cells in a column to any number as this would only require routine skill in the art.)

With regard to **claim 8**, Naiki further discloses an SRAM device as recited in Claim 1 wherein said orientations include first and second opposing orientations (See abstract0 "positional deviations") and said asymmetric memory cells are disposed equally in said first and second orientations (even and odd as shown in figure 9).

Claim 14 is rejected for similar reasons as claim 1. **Claim 15** is rejected for similar reasons as claim 2. **Claim 16** is rejected for similar reasons as claim 3. **Claim 17** is rejected for similar reasons as claim 4. **Claim 19** is rejected for similar reasons as claim 5. **Claim 20** is rejected for similar reasons as claim 7.

If necessary, **claims 9-13**, as far as understood, are also rejected for similar reasons as the corresponding claims rejected above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Najm et al (US PG Pub 2005/0226031, filed in English on 8/8/2003 and claiming US priority to 8/9/2002)

With regard to **claim 21**, Najm discloses an SRAM device (figure 2), comprising:

a first bit line 24;

a second bit line 22; and

a first SRAM cell having a first pass gate connected to said first bit line and a second pass gate N3 wider than said first pass gate N4 connected to said second bitline 22.

(In paragraph 10, it is stated that transistors can be made weaker by decreasing the channel width. Then, in paragraph 34, it is stated that pass transistor N4 is weaker with respect to pass transistor N3. A valid embodiment of the invention of Najm includes a second pass gate N3 wider than a first pass gate N4 as interpreted from claims 1 and 2 shown in the second column of page 8: "a transistor having a decreased channel width as compared to the channel width of the first type of transistor".)

8. Claim 21 is also rejected under 35 U.S.C. 102(e) or 102(a) as being anticipated by Yamauchi (US Patent 6,898,111).

With regard to **claim 21**, Yamauchi discloses an SRAM device (see figures 1 and 2), comprising:

a first bit line WBL;

a second bit line RBL; and

a first SRAM cell (fig. 1) having a first pass gate MN2 connected to said first bit line WBL and a second pass gate MN3 wider than said first pass gate N4 connected to said second bitline RBL. (see table of fig. 2)

9. Claims 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Naiki (US Patent 5,446,699).

Note that "SRAM sense amplifier" has been given no patentable weight as it is in the preamble. Also these claims are rejected for similar reasons as the claims rejected above under 35 U.S.C. 103.

With regard to **claim 9**, Naiki discloses an SRAM device, comprising:

sensing circuitry (87 in figure 11, 81/82 in figure 10, *or* sensing circuitry is considered inherently connected to the data-line pair as discussed below) configured to sense stored values in a column of asymmetric SRAM cells (They have a "positional deviation". See col. 2, lines 6-14.) spanning opposing bit lines (bit line pairs 48 or 49 in fig. 9) in alternating orientations (See col 2, lines 6-36. Odd rows comprise one orientation while even rows comprise the other orientation.); and

switching circuitry (the decoder and logic gates in figures 10, 11, or 12 which inherently comprise switches) configured to apply voltage signals to said sensing circuitry as a function of said orientations. (ie a function of the LSB X1 of the row address as taught in col. 9, lines 22-31)

With regard to **claim 10**, Naiki discloses an SRAM device as recited in Claim 9 wherein

said column has only two of said opposing bit lines.

With regard to **claim 11**, Naiki discloses an SRAM device as recited in Claim 9 wherein said voltage signals comprise different voltage signals (Only one of Co or Ce in figure 10 or adjacent bit lines in other embodiments is high at a time) and said ~~dummy bit line~~ switching circuitry is configured to apply said different voltage signals to opposing sides of said sensing circuitry. (See 82 of figure 10- Signal lines are connected to opposing sides.)

With regard to **claim 12**, Naiki discloses an SRAM device as recited in Claim 9 wherein said orientations alternate based on a power of two. (Even/odd, as shown in the abstract, fits this formula.)

With regard to **claim 13**, Naiki discloses an SRAM device as recited in Claim 9 wherein said switching circuitry (column decoder and logic gates) is configured to receive a signal X1 representing said orientations (even/odd) from a line of an address bus associated with said SRAM cells. (see Row address LSB in figures 10-12)

Allowable Subject Matter

10. Claims 5, 18, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

With regard to **claim 5 and 18**, the prior art does not teach or suggest the SRAM device of claim 1 or method of claim 14 wherein said orientations are based on

threshold voltages of transistors in said cells, *in combination with the other limitations of the claim.*

With regard to **claim 22**, the prior art does not teach or suggest a second SRAM cell oriented opposite to the first, *in combination with all limitations of the claim.*

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Weinberg whose telephone number is 571-272-6424. The examiner can normally be reached on M-F 9:00 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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